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Converting DSP56001-Based Designs to the DSP56002

This document details the differences between the DSP56001 and DSP56002 that need to be taken into consideration when redesigning a system based on the DSP56001 to use the DSP56002. The differences fall into two major categories: changes which must be addressed by the user and enhancements which the designer may elect to implement.

Please refer to the DSP56001 and DSP56002 Technical Data Sheets and their associated documentation for complete information. A list of all associated documents is contained in Appendix A.

1. REQUIRED CHANGES

1.1 Hardware/Layout

1.1.1. Pinout

The physical pinout of the DSP56001 is different from the DSP56002. This means that it is not possible to directly replace a DSP56001 with a DSP56002 without changing the board layout. Please refer to the DSP56002 Technical Data Sheet for details of the device pinout. For comparison purposes, Appendix B of this document contains a table comparing the pin assignments of the DSP56001 packages to the DSP56002 packages.

1.1.2. Packaging

The DSP56001 is available in 3 package types:	PGA, 88 pin
	PQFP, 132 pin
	CQFP, 132 pin
The DSP56002 is also available in 3 package types:	PGA, 132 pin
	PQFP, 132 pin
	TQFP, 144 pin

Note that the PQFP has plastic “tabs” located at each corner. The layout must accommodate these “tabs” and avoid placing components in areas occupied by these “tabs”.

1.1.3. Phase Locked Loop (PLL)

The 56002 has a Phase Locked Loop on-chip which permits operating the device from low frequency external clock sources, precluding the need for additional high frequency clocks exclusively for the high speed DSP. Tying the PINIT to GND disables the PLL upon power up. Although not necessary, the PCAP pin should be tied to Vcc or GND.

1.1.4. OnCE™ Port

The OnCE™ Port has been added to permit unobtrusive access to the core for debugging and testing. Tying the Debug Request (DR#)[1] pin to Vcc will disable the OnCE port. It is recommended that DSCK be tied to GND through a 56k ohm resistor.

1.1.5. Bus Control

There have been several changes made to the bus control pins. The BR# / WT# and BG# / BS# pins on the DSP56001 have been demultiplexed on the DSP56002, and an additional control signal Bus Needed (BN#) has been added.

DSP56001		DSP56002	
input	BR#/WT#	input	BR#
		input	WT#
output	BG#/BS#	output	BG#
		output	BS#
		output	BN#

DSP56001-based designs should be simplified due to the presence of individual signal pins for all bus arbitration functions. Both BR# and WT# require pull-up resistors to Vcc or they must be connected to external logic which assures that their quiescent state is a logic “high”.

1.1.6. Bootstrap

The DSP56002 has an extra Mode Select pin (MODC / NMI#) which also serves as the Non-Maskable Interrupt. The Mode Select pins are read as the processor comes out of reset and are used to define the chip’s operating mode. Refer to the DSP56002 documentation for specific details on the various bootstrap selections available via the MODA / MODB / MODC pins.

The reset circuitry will need to be modified for the DSP56002 so that the device will enter the correct operating mode after exiting reset. For the DSP56002, bit 23 of the data bus no longer serves to select between EPROM and Host Interface Boot modes.

1.1.7. Non-Maskable Interrupt (NMI)

A Non-Maskable Interrupt (NMI) function was previously accessible on the DSP56001 by applying 10 Volts to the MODB / IRQB# pin. The DSP56002 supports a non-maskable interrupt (NMI) through the MODC / NMI# pin which is TTL / CMOS compatible. **DO NOT APPLY 10 VOLTS TO ANY PIN OF THE DSP56002 (including MODB)!** Subjecting any pin of the DSP56002 to voltages in excess of the specified TTL / CMOS levels will permanently damage the device.

1.1.8. DC Electrical Characteristics

The supply voltage and logic level specifications of the DSP56001 and DSP56002 are the same. Most DSP56002 buffers are capable of sinking 3.2 mA compared to the 1.6 mA buffers of the DSP56001. Please refer to the DSP56001 and DSP56002 Technical Data Sheets for specific details.

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[1] Note that throughout this document, # is used to indicate that the signal is asserted when the voltage = ground (active low).

1.1.9. AC Electrical Characteristics

The timing specifications of the DSP56002 differ from those of the DSP56001. This is due, in part, to the superior performance inherent in the design of the DSP56002. The user should evaluate the impact of these differences on a case-by-case basis.

The DSP56002 has been designed to operate at higher frequencies than the DSP56001. As a result, many DSP56002 signals exhibit faster rise- and fall-times than the same signals on the DSP56001. These faster edges may generate more radiated noise and EMI, and may require more attention to these issues (e.g., the DSP56002 based circuit may require better decoupling). Use of the PLL, however, may reduce the actual radiated noise and EMI. Please refer to the DSP56002 documentation.

1.2 Software/Application

The DSP56002 instruction set is upwardly compatible with the DSP56001. This means that software written for the DSP56001 will generally run unmodified on the DSP56002. There are, however, certain differences which result from the DSP56002's enhanced functionality and increased level of performance. Users should consider the impact these differences may have on each application.

1.2.1. MOVEP to Rn/Nn/Mn Registers

On the DSP56001 there is a pipeline delay when using the MOVEP instruction to change the contents of an address register (Mn, Nn, or Rn). The new contents of the destination address register will not be available for use during the following instruction (i.e, there is a single instruction cycle delay).

On the DSP56002 this pipeline delay has been removed. If an address register (Mn, Nn, or Rn) is directly changed with a MOVEP instruction, the updated contents will be available for use during the following instruction. DSP56001 software which depends on this pipeline delay must be modified when moved onto the DSP56002.

1.2.2. MOVEP to/from Data ALU Registers

MOVEP Instructions to / from Data ALU Registers take 2 instruction cycles on the DSP56001. On the DSP56002, these instructions take only 1 instruction cycle. DSP56001 software which is dependent on the timing of this form of the MOVEP instruction must be modified when ported to the DSP56002.

1.2.3. MOVEP Immediate

MOVEP Immediate instructions take 3 instruction cycles on the DSP56001. On the DSP56002, these instructions take only 2 instruction cycles. DSP56001 software which is dependent on the timing of this form of the MOVEP instruction must be modified when ported to the DSP56002.

1.2.4. Stop/Wait Timing

Wake-up from the Stop and Wait operating modes with IRQn# is longer on the DSP56002 by one Tc period.

1.2.5. SCI/SSI Initialization Timing

On the DSP56002, the SCI and SSI clocks are stopped when the peripherals are not enabled in order to save power. As a result, the initialization time of the SCI and SSI is longer on the DSP56002.

1.2.6. Control Registers

The DSP56002 has been improved to support Block Floating Point, Double Precision Arithmetic, additional bootstrap modes, NMI and other features. In order to support these improvements, the OMR and the Status Register have been altered, as outlined in Table 1.

Table 1: Summary of Control Register Differences

Register	Bit	DSP56001 Definition	DSP56002 Definition	Explanation of Difference
Status Register	7	Reserved - Read/Written as zero.	S - Scaling bit	On the 002 this bit can be read as '1' depending on the contents of S1,S0, and the accumulators. It is a sticky bit.
	13	T - Trace mode	T - Trace mode	The 002 manual states that the OnCE trace mode should be used.
	14	Reserved - Read/Written as zero.	DM - Double precision multiply	In the 002, if the DM bit is set, the operations performed by the MPY and MAC instructions change.
Operating Mode Register	0,1,4	0 - MA 1 - MB 4 - Reserved	0 - MA 1 - MB 4 - MC	These three bits control the operating mode of the device. The MODA, B & C pins are latched in on reset. Completely different for 001 and 002.
	3	Reserved - Read/Written as zero.	YD - internal Y memory disable	If this bit is set, all Y memory data addresses are considered to be external.
	7	EA - External memory access	Reserved - Read/Written as zero.	Controls the definition of the Port A control pins. Not required on the 002 as the bus control pins have been de-multiplexed.

1.2.7. X:Memory Mapped Peripheral Registers

In order to support the new peripherals present on the DSP56002, some of the reserved X:I/O addresses which were reserved on the DSP56001 have been redefined as peripheral control registers. It is important to ensure that the new definitions of these previously unused X:I/O addresses do not conflict with any software developed for the DSP56001.

Many of the peripheral control registers within the DSP56001 and DSP56002 have reserved bits. Reads from these reserved bits will return zero. In order to guarantee compatibility with future products, these bits should be written as zero. On the DSP56002, some of the previously reserved bits in these registers have been redefined in order to support enhanced funtionality.

Table 2 shows all the differences between the DSP56001 and DSP56002 memory mapped peripheral registers.

Table 2: Summary of Memory Mapped Register Differences

Register	Bit	DSP56001 Definition	DSP56002 Definition	Explanation of Difference
PLL Control Register X:$FFFD	All	Reserved - read as random, write as don't care.	Control the operation of the PLL	This address should not have been used on the 001. Users will have to ensure that this is the case.
OnCE GDB Register X:$FFFC	All	Reserved - read as random, write as don't care.	Used in the execution of OnCE commands	This address should not have been used on the 001. Users will have to ensure that this is the case.
SCI Interface Control Register (SCR) X:$FFF0	14	Written as zero in the manual	STIR - Timer interrupt rate	On the 001 this bit should be written as zero. If this bit has been written as '1' it will increase the timer resolution on the 002 by 32 times.
Port B Control Register (PBC) X:$FFE0	1	Written as zero in manual	Offers additional options for host interface	If written as zero, as described in the manual, will cause no problems. If written as '1' either the HACK# pin will be GPIO, or the register will contain an invalid value (depending on the state of bit 0)
Timer Control Registers X:$FFDF X:$FFDE	All	Reserved - read as random, write as don't care.	Control Registers for the Timer	These addresses should not have been used on the 001. If they have, it may effect the operation of the timer on the 002.

1.3 Host Command Vector Register

The DSP56002 supports 64 Interrupt Vectors, compared to the 32 Interrupt Vectors supported by the DSP56001.

Table 3: Summary of Host Command Vector Register Differences

Register	Bit	DSP56001 Definition	DSP56002 Definition	Explanation of Difference
Host Command Vector Register (CVR)	5	Reserved - read as zero, written as zero.	Host Vector MSB	This bit should always be written as zero on the 001. Setting this bit on the DSP56002 permits selection of one of the second group of 32 Interrupt Vectors.

2. ENHANCEMENTS

The DSP56002 embodies numerous improvements to the DSP56001 design. Users migrating from the DSP56001 may wish to take advantage of these enhancements in their new designs.

2.1 Hardware/Layout

2.1.1. Clock Speed / Performance

The DSP56001 is available in 20.5 MHz, 27 MHz and 33 MHz versions. There are no planned speed improvements beyond 33 MHz.

The DSP56002 is available in 40 MHz and 66 MHz versions. Faster speeds are planned.

2.1.2. Power Consumption

The DSP56002 consumes less power than the DSP56001. In addition, a low voltage version of the DSP56002 is available; the DSP56L002 operates from 3.3 volt power sources. Refer to the DSP56002/L002 Technical Data Sheet.

2.1.3. Fully Static Operation

The DSP56002 is a fully static device, capable of operation down to DC.

2.1.4. Clock Out Pin (CKOUT)

The CKOUT pin of the DSP56002 provides the user with a clock source which can be driven by either the core clock or the output of a Low Power Divider (LPD). This signal has been designed to minimize skew between external peripheral clocks and the core.

2.1.5. Phase Locked Loop (PLL)

The PLL is a new feature that has been added to the DSP56002. It allows the DSP56002 to be driven by a low frequency external clock which is multiplied up on chip to allow full frequency operation. There are 9 pins dedicated to the PLL.

	DSP56002	
PLL	supply	Vccp
	supply	GNDP
	input	PCAP
	input	CKP
	output	PLOCK
	supply	Vcccl
	supply	GNDCL
	input	PINIT
	output	CKOUT

2.1.6. OnCE™ Port

The On-Chip Emulator (OnCE) interface has been added to the DSP56002. This is a debug feature that allows access to all registers. There are 4 pins dedicated to the OnCE interface.

	DSP56002	
OnCE	in/out	DSCK/OS1
	in/out	DSI/OS0
	input	DR#
	output	DSO

2.1.7. Host Acknowledge (HACK#)

The HACK# pin may now be used as a general purpose I/O pin (GPIO) independent of the other Host Interface pins. Bits 0 and 1 of the Port B Control Register (PBC) now work in concert to define the function of HACK# and the remaining Host Interface Pins.

2.1.8. Timer/TIO Pin

A 24-bit timer/event counter has been added to the DSP56002. Refer to the DSP56002 User's Manual, Section 7, Timer and Event Counter.

2.1.9. I/O Buffer Drive

Most DSP56002 buffers are capable of sinking 3.2 mA compared to the 1.6 mA buffers of the DSP56001. Refer to the DSP56002 Technical Data Sheet.

2.1.10. SCI Timer Interrupt Rate

Bit 14 in the SCI Control Register now controls a divide by 32 in the SCI Timer interrupt generator. This bit was reserved on the DSP56001.

2.1.11. SCI Bootstrap

The 56002 supports bootstrapping from the SCI.

2.1.12. Demultiplexed Bus Control Signals

As mentioned above, BR#, BG#, BS# and WT# no longer share pins. On the DSP56002, the bus arbitration function and the external wait state generation function are no longer mutually exclusive. In addition, a new pin, Bus Needed (BN#) has been added.

2.2 Software/Application

2.2.1. MOVEP Timing

Refer to the discussion above regarding enhanced performance of the MOVEP instructions.

2.2.2. Double Precision Multiply

Refer to the DSP56000 Family Manual, Section 3, Data Arithmetic Logic Unit.

2.2.3. Wrap Around Addressing Mode

Refer to the DSP56000 Family Manual, Section 4, Address Generation Unit and Addressing Modes.

2.2.4. Block Floating Point

Refer to the DSP56000 Family Manual, Section 5, Program Control Unit, Section 5.4.2, Status Register.

2.2.5. Increased Vector Table Size

The DSP56001 supports 32 interrupt vectors (P:$00-P:$3F) while the DSP56002 supports 64 vectors (P:$00-P:$7F).

2.2.6. Host Command Register

The Host Vector portion of the Host Command Register (HCR) has been extended to 6 bits in order to support the increased vector table size.

2.2.7. Instruction Set Enhancements

The following Instructions have been added:

INC
DEC
DEBUG
DEBUGcc
Immediate versions of MPY/MPYR/MAC/MACR

Refer to the DSP56000 Family Manual, Appendix A, Instruction Set Details.

APPENDIX A - Related Documents

Complete technical information on the DSP56001 and DSP56002 is contained in the following documents, which can be ordered from your Motorola Literature Distribution Center using the reference numbers shown:

DSP56001 Technical Data Sheet - DSP56001/D
DSP56000/1 Users Manual - DSP56000UM/AD
DSP56002 Technical Data Sheet - DSP56002/D
DSP56000 Family Manual - DSP56KFAM/D
DSP56002 Users Manual - DSP56002UM/AD

APPENDIX B - Comparison of DSP56001 to DSP56002 Pin Assignments

Table 4: Signal Name to DSP56001 and DSP56002 Pinout Cross Reference

Signal Name	DSP56001 FC or FE 132 pin PQFP or CQFP Pin	DSP56002 FC 132 pin PQFP Pin	DSP56002 PV 144 pin TQFP Pin	DSP56001 RC 88 pin PGA Pin	DSP56002 RC 132 pin PGA Pin
A0	53	60	83	M11	K9
A1	54	61	84	N11	L9
A2	57	63	86	N10	M9
A3	58	64	87	M9	L8
A4	60	65	88	N9	M8
A5	61	68	92	M8	M7
A6	65	71	95	N8	L7
A7	67	72	96	N7	M6
A8	68	73	97	N6	L6
A9	70	74	98	M6	M5
A10	71	76	100	N5	L5
A11	75	77	101	M5	K5
A12	76	78	102	N4	M4
A13	77	80	104	N3	L4
A14	79	82	106	N2	K4
A15	80	83	107	M3	J4
BG#	43	43	64	K12	K12
BN#		41	62		H13
BR#	45	44	65	L13	L12
BS#	43	54	77	K12	N11
CKOUT		123	8		C5
CKP		126	11		B4
D0	81	84	110	N1	N2
D1	82	85	111	M2	M3
D2	85	87	113	L2	M2
D3	86	88	114	M1	L3
D4	87	90	116	L1	L2
D5	88	91	117	K2	K3
D6	92	93	119	K1	K2
D7	93	94	120	J2	J3
D8	94	95	121	J1	J2
D9	96	96	122	H1	H3
D10	97	100	126	G1	H2

D11	99	101	128	F1	H1
D12	102	103	130	F2	G3
D13	104	104	131	E1	G2
D14	105	106	133	D1	G1
D15	106	107	134	C1	F1
D16	108	108	135	D2	F2
D17	109	109	136	B1	F3
D18	113	111	138	C2	E2
D19	114	112	139	A1	E3
D20	115	114	141	B2	D2
D21	118	115	142	A2	D3
D22	119	117	2	A3	E4
D23	120	118	3	B4	D4
DR#		51	74		K11
DS#	49	57	80	M12	L10
DSCK		50	71		N12
DSI		53	76		M11
DSO		52	75		L11
EXTAL	127	1	19	B6	C8
GNDC		48	69		N13
GNDCK		122	7		C4
GNDD	90	86	112	D3	B1
GNDD	91	92	118	J3	D1
GNDD	111	99	125		E1
GNDD	112	105	132		K1
GNDD		110	137		L1
GNDD		116	143		N1
GNDH	23	5	23	E11	A12
GNDH	24	11	29		A13
GNDH		16	34		C13
GNDH		22	42		E13
GNDN	55	56	79	L6	N10
GNDN	56	62	85	L9	N3
GNDN	73	70	94		N5
GNDN	74	75	99		N6
GNDN		81	105		N8
GNDP		129	14		C6
GNDQ	33	3	21	B7	A1
GNDQ	34	36	57	G11	A3
GNDQ	130	67	90		A5
GNDQ	131	98	124		A7
GNDS		27	47		J13
GNDS		34	54		L13
H0	25	24	44	D12	E11

H1	22	23	43	C13	D11
H2	20	21	41	C12	C11
H3	19	19	39	B13	E10
H4	16	18	38	B12	D10
H5	15	17	35	A13	B12
H6	14	15	33	A12	A11
H7	11	14	32	B11	B11
HA0	5	7	25	B8	C9
HA1	2	6	24	A8	B9
HA2	1	4	22	A7	A9
HACK#	6	8	26	A9	A10
HEN#	8	10	28	A10	B10
HR/W#	9	12	30	A11	D9
HREQ#	10	13	31	B10	C10
IRQA#	123	121	6	B5	C3
IRQB#	121	120	5	A4	C2
MODA	123	121	6	B5	C3
MODB	121	120	5	A4	C2
MODC		119	4		D5
NMI#*	121	119	4	A4	D5
OS0		53	76		M11
OS1		50	71		N12
PB0	25	24	44	D12	E11
PB1	22	23	43	C13	D11
PB2	20	21	41	C12	C11
PB3	19	19	39	B13	E10
PB4	16	18	38	B12	D10
PB5	15	17	35	A13	B12
PB6	14	15	33	A12	A11
PB7	11	14	32	B11	B11
PB8	5	7	25	B8	C9
PB9	2	6	24	A8	B9
PB10	1	4	22	A7	A9
PB11	9	12	30	A11	D9
PB12	8	10	28	A10	B10
PB13	10	13	31	B10	C10
PB14	6	8	26	A9	A10
PC0	27	25	45	D13	C12
PC1	28	26	46	E13	D12
PC2	29	28	48	F13	E12
PC3	31	29	49	F12	F11
PC4	40	35	56	K13	G12
PC5	37	32	52	H13	F13
PC6	32	31	51	G13	F12

PC7	42	38	59	J12	G13
PC8	39	33	53	J13	G11
PCAP		128	13		B6
PINIT		131	16		C7
PLOCK		130	15		B7
PS#	52	59	82	N12	M10
RD#	47	47	68	L12	J10
RESET#	124	125	10	A5	B3
RXD	27	25	45	D13	C12
SC0	31	29	49	F12	F11
SC1	40	35	56	K13	G12
SC2	37	32	52	H13	F13
SCK	32	31	51	G13	F12
SCLK	29	28	48	F13	E12
SRD	42	38	59	J12	G13
STD	39	33	53	J13	G11
TIO		39	60		H11
TXD	28	26	46	E13	D12
VCCC		45	66		M13
VCCCK		124	9		B2
VCCD	100	89	115	G3	C1
VCCD	101	102	129		J1
VCCD		113	140		M1
VCCH	12	9	27	C9	B13
VCCH	13	20	40		D13
VCCN	63	58	81	L8	N4
VCCN	64	69	93		N7
VCCN		79	103		N9
VCCP		127	12		B5
VCCQ	35	2	20	C6	A2
VCCQ	36	37	58	G12	A4
VCCQ	128	66	89		A6
VCCQ	129	97	123		A8
VCCS		30	50		K13
WR#	46	46	67	M13	J11
WT#	45	42	63	L13	J12
X/Y#	48	55	78	N13	K10
XTAL	126	132	17	A6	B8
nc	3	40	1		H12
nc	4	49	18		M12
nc	7		36		
nc	17		37		
nc	18		55		
nc	21		61		

nc	26		70		
nc	30		72		
nc	38		73		
nc	41		91		
nc	44		108		
nc	50		109		
nc	51		127		
nc	59		144		
nc	62				
nc	66				
nc	69				
nc	72				
nc	78				
nc	83				
nc	84				
nc	89				
nc	95				
nc	98				
nc	103				
nc	107				
nc	110				
nc	116				
nc	117				
nc	122				
nc	125				
nc	132				

Notes:

# indicates the signal is asserted when the voltage = ground (active low).

* On the 56001 (only): NMI is a 10 V high signal, BR# also acts as WT#, and BG# also acts as BS# .

nc = no connection.

Table 5: Pinout to DSP56001 and DSP56002 Signal Name Cross Reference

DSP56001 FC or FE 132 pin PQFP or CQFP Pin	DSP56002 FC 132 pin PQFP Pin	DSP56002 PV 144 pin TQFP Pin	Signal Name
1	4	22	HA2/PB10
2	6	24	HA1/PB9
3	40	61	nc
4	49	70	nc
5	7	25	HA0/PB8
6	8	26	HACK#/PB14
7		91	nc
8	10	28	HEN#/PB12
9	12	30	HR/W#/PB11
10	13	31	HREQ#/PB13
11	14	32	H7/PB7
12	20	40	VCCH
13	9	27	VCCH
14	15	33	H6/PB6
15	17	35	H5/PB5
16	18	38	H4/PB4
17		108	nc
18		109	nc
19	19	39	H3/PB3
20	21	41	H2/PB2
21		127	nc
22	23	43	H1/PB1
23	16	34	GNDH
24	22	42	GNDH
25	24	44	H0/PB0
26		73	nc
27	25	45	RXD/PC0
28	26	46	TXD/PC1
29	28	48	SCLK/PC2
30		18	nc
31	29	49	SC0/PC3
32	31	51	SCK/PC6
33	3	21	GNDQ
34	36	57	GNDQ
35	37	58	VCCQ
36	2	20	VCCQ
37	32	52	SC2/PC5
38		55	nc

39	33	53	STD/PC8
40	35	56	SC1/PC4
41		72	nc
42	38	59	SRD/PC7
43	43	64	BG#(/BS#)*
44			nc
45	44	65	BR#(/WT#)*
46	46	67	WR#
47	47	68	RD#
48	55	78	X/Y#
49	57	80	DS#
50		144	nc
51		1	nc
52	59	82	PS#
53	60	83	A0
54	61	84	A1
55	70	94	GNDN
56	62	85	GNDN
57	63	86	A2
58	64	87	A3
59			nc
60	65	88	A4
61	68	92	A5
62			nc
63	79	103	VCCN
64	69	93	VCCN
65	71	95	A6
66			nc
67	72	96	A7
68	73	97	A8
69			nc
70	74	98	A9
71	76	100	A10
72			nc
73	75	99	GNDN
74	81	105	GNDN
75	77	101	A11
76	78	102	A12
77	80	104	A13
78			nc
79	82	106	A14
80	83	107	A15
81	84	110	D0
82	85	111	D1

83		36	nc
84		37	nc
85	87	113	D2
86	88	114	D3
87	90	116	D4
88	91	117	D5
89			nc
90	99	125	GNDD
91	92	118	GNDD
92	93	119	D6
93	94	120	D7
94	95	121	D8
95			nc
96	96	122	D9
97	100	126	D10
98			nc
99	101	128	D11
100	113	140	VCCD
101	102	129	VCCD
102	103	130	D12
103			nc
104	104	131	D13
105	106	133	D14
106	107	134	D15
107			nc
108	108	135	D16
109	109	136	D17
110			nc
111	105	132	GNDD
112	110	137	GNDD
113	111	138	D18
114	112	139	D19
115	114	141	D20
116			nc
117			nc
118	115	142	D21
119	117	2	D22
120	118	3	D23
121	120	5	MODB/IRQB#(NMI/)*
122			nc
123	121	6	MODA/IRQA#
124	125	10	RESET#
125			nc
126	132	17	XTAL

127	1	19	EXTAL
128	97	123	VCCQ
129	66	89	VCCQ
130	67	90	GNDQ
131	98	124	GNDQ
132			nc
	5	23	GNDH
	11	29	GNDH
	27	47	GNDS
	30	50	VCCS
	34	54	GNDS
	39	60	TIO
	41	62	BN#
	42	63	WT#
	45	66	VCCC
	48	69	GNDC
	50	71	DSCK/OS1
	51	74	DR#
	52	75	DSO
	53	76	DSI/OS0
	54	77	BS#
	56	79	GNDN
	58	81	VCCN
	86	112	GNDD
	89	115	VCCD
	116	143	GNDD
	119	4	MODC/NMI#*
	122	7	GNDCK
	123	8	CKOUT
	124	9	VCCCK
	126	11	CKP
	127	12	VCCP
	128	13	PCAP
	129	14	GNDP
	130	15	PLOCK
	131	16	PINIT

Notes:
# indicates the signal is asserted when the voltage = ground (active low).
* NMI is a 10 V high signal on the 56001 (only).
nc = no connection.

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'001  '002  '002                  '001  '002  '002
FC/FE   FC    PV     Signal       FC/FE   FC    PV     Signal
 132   132   144                   132   132   144
```

PQFP/ CQFP Pin	PQFP Pin	TQFP Pin	Name		PQFP/ CQFP Pin	PQFP Pin	TQFP Pin	Name
1	4	22	HA2/PB10	:	84		37	nc
2	6	24	HA1/PB9	:	85	87	113	D2
3	40	61	nc	:	86	88	114	D3
4	49	70	nc	:	87	90	116	D4
5	7	25	HA0/PB8	:	88	91	117	D5
6	8	26	HACK#/PB14	:	89			nc
7		91	nc	:	90	99	125	GNDD
8	10	28	HEN#/PB12	:	91	92	118	GNDD
9	12	30	HR/W#/PB11	:	92	93	119	D6
10	13	31	HREQ#/PB13	:	93	94	120	D7
11	14	32	H7/PB7	:	94	95	121	D8
12	20	40	VccH	:	95			nc
13	9	27	VccH	:	96	96	122	D9
14	15	33	H6/PB6	:	97	100	126	D10
15	17	35	H5/PB5	:	98			nc
16	18	38	H4/PB4	:	99	101	128	D11
17		108	nc	:	100	113	140	VccD
18		109	nc	:	101	102	129	VccD
19	19	39	H3/PB3	:	102	103	130	D12
20	21	41	H2/PB2	:	103			nc
21		127	nc	:	104	104	131	D13
22	23	43	H1/PB1	:	105	106	133	D14
23	16	34	GNDH	:	106	107	134	D15
24	22	42	GNDH	:	107			nc
25	24	44	H0/PB0	:	108	108	135	D16
26		73	nc	:	109	109	136	D17
27	25	45	RXD/PC0	:	110			nc
28	26	46	TXD/PC1	:	111	105	132	GNDD
29	28	48	SCLK/PC2	:	112	110	137	GNDD
30		18	nc	:	113	111	138	D18
31	29	49	SC0/PC3	:	114	112	139	D19
32	31	51	SCK/PC6	:	115	114	141	D20
33	3	21	GNDQ	:	116			nc
34	36	57	GNDQ	:	117			nc
35	37	58	VccQ	:	118	115	142	D21
36	2	20	VccQ	:	119	117	2	D22
37	32	52	SC2/PC5	:	120	118	3	D23
38		55	nc	:	121	120	5	MODB/IRQB#(NMI/)*
39	33	53	STD/PC8	:	122			nc
40	35	56	SC1/PC4	:	123	121	6	MODA/IRQA#
41		72	nc	:	124	125	10	RESET#
42	38	59	SRD/PC7	:	125			nc
43	43	64	BG#(/BS#)*	:	126	132	17	XTAL

44			nc	: 127	1	19	EXTAL
45	44	65	BR#(/WT#)*	: 128	97	123	VccQ
46	46	67	WR#	: 129	66	89	VccQ
47	47	68	RD#	: 130	67	90	GNDQ
48	55	78	X/Y#	: 131	98	124	GNDQ
49	57	80	DS#	: 132			nc
50		144	nc	:	5	23	GNDH
51		1	nc	:	11	29	GNDH
52	59	82	PS#	:	27	47	GNDS
53	60	83	A0	:	30	50	VccS
54	61	84	A1	:	34	54	GNDS
55	70	94	GNDN	:	39	60	TIO
56	62	85	GNDN	:	41	62	BN#
57	63	86	A2	:	42	63	WT#
58	64	87	A3	:	45	66	VccC
59			nc	:	48	69	GNDC
60	65	88	A4	:	50	71	DSCK/OS1
61	68	92	A5	:	51	74	DR#
62			nc	:	52	75	DSO
63	79	103	VccN	:	53	76	DSI/OS0
64	69	93	VccN	:	54	77	BS#
65	71	95	A6	:	56	79	GNDN
66			nc	:	58	81	VccN
67	72	96	A7	:	86	112	GNDD
68	73	97	A8	:	89	115	VccD
69			nc	:	116	143	GNDD
70	74	98	A9	:	119	4	MODC/NMI# *
71	76	100	A10	:	122	7	GNDCK
72			nc	:	123	8	CKOUT
73	75	99	GNDN	:	124	9	VccCK
74	81	105	GNDN	:	126	11	CKP
75	77	101	A11	:	127	12	VccP
76	78	102	A12	:	128	13	PCAP
77	80	104	A13	:	129	14	GNDP
78			nc	:	130	15	PLOCK
79	82	106	A14	:	131	16	PINIT
80	83	107	A15				
81	84	110	D0				
82	85	111	D1				
83		36	nc				

Notes:
# indicates the signal is asserted when the voltage = ground (active low).
* On the 56001 (only): NMI is a 10 V high signal, BR# also acts as WT#, and BG# also acts as BS#.
nc = no connection.

Signal Name	'001 FC/FE 132 pin PQFP/ CQFP Pin	'002 FC 132 pin PQFP Pin	'002 PV 144 pin TQFP Pin	'001 RC 88 pin PGA Pin	'002 RC 132 pin PGA Pin
A0	53	60	83	M11	K9
A1	54	61	84	N11	L9
A2	57	63	86	N10	M9
A3	58	64	87	M9	L8
A4	60	65	88	N9	M8
A5	61	68	92	M8	M7
A6	65	71	95	N8	L7
A7	67	72	96	N7	M6
A8	68	73	97	N6	L6
A9	70	74	98	M6	M5
A10	71	76	100	N5	L5
A11	75	77	101	M5	K5
A12	76	78	102	N4	M4
A13	77	80	104	N3	L4
A14	79	82	106	N2	K4
A15	80	83	107	M3	J4
BG#	43	43	64	K12	K12
BN#		41	62		H13
BR#	45	44	65	L13	L12
BS#	43	54	77	K12	N11
CKOUT		123	8		C5
CKP		126	11		B4
D0	81	84	110	N1	N2
D1	82	85	111	M2	M3
D2	85	87	113	L2	M2
D3	86	88	114	M1	L3
D4	87	90	116	L1	L2
D5	88	91	117	K2	K3
D6	92	93	119	K1	K2
D7	93	94	120	J2	J3
D8	94	95	121	J1	J2
D9	96	96	122	H1	H3
D10	97	100	126	G1	H2
D11	99	101	128	F1	H1
D12	102	103	130	F2	G3
D13	104	104	131	E1	G2
D14	105	106	133	D1	G1

D15	106	107	134	C1	F1
D16	108	108	135	D2	F2
D17	109	109	136	B1	F3
D18	113	111	138	C2	E2
D19	114	112	139	A1	E3
D20	115	114	141	B2	D2
D21	118	115	142	A2	D3
D22	119	117	2	A3	E4
D23	120	118	3	B4	D4
DR#		51	74		K11
DS#	49	57	80	M12	L10
DSCK		50	71		N12
DSI		53	76		M11
DSO		52	75		L11
EXTAL	127	1	19	B6	C8
GNDC		48	69		N13
GNDCK		122	7		C4
GNDD	90	86	112	D3	B1
GNDD	91	92	118	J3	D1
GNDD	111	99	125		E1
GNDD	112	105	132		K1
GNDD		110	137		L1
GNDD		116	143		N1
GNDH	23	5	23	E11	A12
GNDH	24	11	29		A13
GNDH		16	34		C13
GNDH		22	42		E13
GNDN	55	56	79	L6	N10
GNDN	56	62	85	L9	N3
GNDN	73	70	94		N5
GNDN	74	75	99		N6
GNDN		81	105		N8
GNDP		129	14		C6
GNDQ	33	3	21	B7	A1
GNDQ	34	36	57	G11	A3
GNDQ	130	67	90		A5
GNDQ	131	98	124		A7
GNDS		27	47		J13
GNDS		34	54		L13
H0	25	24	44	D12	E11
H1	22	23	43	C13	D11
H2	20	21	41	C12	C11
H3	19	19	39	B13	E10
H4	16	18	38	B12	D10
H5	15	17	35	A13	B12
H6	14	15	33	A12	A11
H7	11	14	32	B11	B11

HA0	5	7	25	B8	C9
HA1	2	6	24	A8	B9
HA2	1	4	22	A7	A9
HACK#	6	8	26	A9	A10
HEN#	8	10	28	A10	B10
HR/W#	9	12	30	A11	D9
HREQ#	10	13	31	B10	C10
IRQA#	123	121	6	B5	C3
IRQB#	121	120	5	A4	C2
MODA	123	121	6	B5	C3
MODB	121	120	5	A4	C2
MODC		119	4		D5
NMI#*	121	119	4	A4	D5
OS0		53	76		M11
OS1		50	71		N12
PB0	25	24	44	D12	E11
PB1	22	23	43	C13	D11
PB2	20	21	41	C12	C11
PB3	19	19	39	B13	E10
PB4	16	18	38	B12	D10
PB5	15	17	35	A13	B12
PB6	14	15	33	A12	A11
PB7	11	14	32	B11	B11
PB8	5	7	25	B8	C9
PB9	2	6	24	A8	B9
PB10	1	4	22	A7	A9
PB11	9	12	30	A11	D9
PB12	8	10	28	A10	B10
PB13	10	13	31	B10	C10
PB14	6	8	26	A9	A10
PC0	27	25	45	D13	C12
PC1	28	26	46	E13	D12
PC2	29	28	48	F13	E12
PC3	31	29	49	F12	F11
PC4	40	35	56	K13	G12
PC5	37	32	52	H13	F13
PC6	32	31	51	G13	F12
PC7	42	38	59	J12	G13
PC8	39	33	53	J13	G11
PCAP		128	13		B6
PINIT		131	16		C7
PLOCK		130	15		B7
PS#	52	59	82	N12	M10
RD#	47	47	68	L12	J10
RESET#	124	125	10	A5	B3
RXD	27	25	45	D13	C12
SC0	31	29	49	F12	F11

SC1	40	35	56	K13	G12
SC2	37	32	52	H13	F13
SCK	32	31	51	G13	F12
SCLK	29	28	48	F13	E12
SRD	42	38	59	J12	G13
STD	39	33	53	J13	G11
TIO		39	60		H11
TXD	28	26	46	E13	D12
VccC		45	66		M13
VccCK		124	9		B2
VccD	100	89	115	G3	C1
VccD	101	102	129		J1
VccD		113	140		M1
VccH	12	9	27	C9	B13
VccH	13	20	40		D13
VccN	63	58	81	L8	N4
VccN	64	69	93		N7
VccN		79	103		N9
VccP		127	12		B5
VccQ	35	2	20	C6	A2
VccQ	36	37	58	G12	A4
VccQ	128	66	89		A6
VccQ	129	97	123		A8
VccS		30	50		K13
WR#	46	46	67	M13	J11
WT#	45	42	63	L13	J12
X/Y#	48	55	78	N13	K10
XTAL	126	132	17	A6	B8
nc	3	40	1		H12
nc	4	49	18		M12
nc	7		36		
nc	17		37		
nc	18		55		
nc	21		61		
nc	26		70		
nc	30		72		
nc	38		73		
nc	41		91		
nc	44		108		
nc	50		109		
nc	51		127		
nc	59		144		
nc	62				
nc	66				
nc	69				
nc	72				
nc	78				

nc	83
nc	84
nc	89
nc	95
nc	98
nc	103
nc	107
nc	110
nc	116
nc	117
nc	122
nc	125
nc	132

Notes:
# indicates the signal is asserted when the voltage = ground (active low).
* NMI is a 10 V high signal on the 56001 (only).
nc = no connection.

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